REMARKS

Applicants acknowledge receipt of the Examiner's Office Action dated July 18, 2006. This Office Action rejected all claims pending at the time. In light of the foregoing amendments and following remarks, Applicants respectfully request the Examiner's reconsideration and reexamination of all pending claims.

Claim 15 stands rejected under 35 U.S.C. § 102(a) as being anticipated by Figure 1-2 of the PCI Express™ to PCI/PCI-X Bridge Specification. Claim 15 recites several components formed on a substrate. More particularly, line 15 recites a PCI data bus, a first subcircuit, and a second subcircuit, all formed on the same substrate. Applicants have reviewed Figure 1-2 of PCI Express™ to PCI/PCI-X Bridge Specification and can find no teaching or fair suggestion of a PCI data bus, a first subcircuit, and a second subcircuit all formed on the same substrate, either alone or in combination with the remaining limitations of claim 15. As such, Applicants assert that claim 15 is patentably distinguishable over Figure 1-2 of the PCI Express™ to PCI/PCI-X Bridge Specification.

Claims 1-15 were rejected under 35 U.S.C. § 103 as being unpatentable over the admitted prior art in view of U.S. Patent No. 6,594,712 issued to Christopher Pettey et al. ("Pettey"). For the purposes of this Office Action Response only, Applicants will presume that the Background Section of the instant application is admitted prior art. Independent claim 1 recites a first circuit coupled to a second circuit via a PCI data bus. Claim 1 also recites that the PCI data bus is configured to transmit data between only the first and second circuits. In rejecting independent claim 1, the Office Action asserts the admitted prior art does not teach a PCI data bus which is configured to transmit data between only the first and second circuits.

However, the Office Action asserts that Pettey discloses this missing limitation. Specifically, the Office Action asserts that Pettey discloses claim 1's first circuit (Fig. 2, I/O controller 206) coupled to claim 1's second circuit (Fig. 2, TCA 202). Fig. 2 of Pettey shows a PCI bus-a 216 coupled between I/O controller 206 and TCA 202. However, as more fully described below, PCI bus-a 216 is not configured to transmit data only between TCA 206 and I/O controller 202 as required by claim 1.

Column 7, lines 14-25 of Pettey teaches, "Coupled to one of the PCI buses 216 [sic] is a local CPU 208, for programming the TCA 202 and I/O controllers 206." Also, the cited section of Pettey teaches, "In addition, the local memory 218 may be used to store data from the I/O controllers 206..." Given that CPU 208 is coupled between PCI I/O controller 206 and local memory 218, it follows the PCI bus-a 216 is used for transmitting data between PCI I/O controller 206 and CPU 208 in addition to transmitting data between PCI I/O controller 206 and TCA 202. As such, Applicants assert that claim 1 is patentably distinguishable over the cited sections of Pettey in combination with the cited sections of the admitted prior art.

The remaining independent claims recite the same or similar features argued above. As such, Applicants assert the remaining independent claims are patentably distinguishable over the admitted prior art in view of Pettey.

CONCLUSION

Applicants submit that all claims are now in condition for allowance, and an early notice to that effect is earnestly solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia, 22313-1450, on November 10, 2006.

Attorney for Applicants — Date of Signature: 11/10/06

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